REQUIREMENTS, CHALLENGES AND CURRENT STATUS OF THIN WAFER CARRIER SYSTEMS FOR 3D TSV THINNING AND BACKSIDE PROCESSING

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3DS-IC MANUFACTURING – FROM CONCEPT TO COMMERCIALIZATION

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OVERVIEW

• Need for a thin wafer carrier system?
• Integration in the 3D process flow
• Temporary carrier wafer bonding
• Temporary carrier wafer de-bonding
• Conclusion
TECHNOLOGY MODULES FOR 3D TSV INTEGRATION

3-Main Technology components

- TSV Technology
- Wafer thinning & Thin wafer handling
- Chip stacking & stack packaging
Si WAFER THINNING

Advances in wafer thinning allow wafer thinning down to 50 µm and even less, while maintaining a total thickness variation, TTV < 1 µm.

Thin wafers, below 100 µm become flexible.

Defects at the edge of the wafer cause these wafer to be fragile.
NEED FOR A THIN WAFER SUPPORT SYSTEM DURING 3D PROCESSING

▸ Handling in semiconductor processing tools: compliance to standards and avoiding damage to thin wafers

▸ Front-side device wafer, generally with exposed metal pads, μbump or flip chip bumps, should not be in contact with the tool chucks to avoid damage and contamination.

▸ Thin wafers are very fragile particularly at the edges

40 μm wafer showing stress relaxation

Broken pieces

20 μm
WHICH CARRIER SOLUTIONS?

- Bonding to glass wafers:
  + Transparent carrier: allows for optical debonding techniques (typically laser based)
  - Glass must be SI-CTE matched across a large temperature range
  - Glass must be ground to tight TTV specification (high cost)
  - Not compatible with electrostatic chucks
  - Significant impact of low thermal conductivity and electrically isolating properties of glass on process parameters on post grinding processes
WHICH CARRIER SOLUTIONS?

- Bonding to glass wafers

- Bonding to silicon carriers
  - Highly compatible to semiconductor equipment
  - Readily available with good TTV (low cost: device grade not required)
  - Not transparent: laser-based release methods not applicable

- Carrier-less system: “Tyco”
WHICH CARRIER SOLUTIONS?

- Bonding to glass wafers
- Bonding to silicon carriers
- Bonding to perforated silicon (or glass) carriers
  - Allows for a solvent release method
  - Expensive carrier substrate
  - Holes result in local thickness variations on carrier wafers
WHICH CARRIER SOLUTIONS?

- Bonding to glass wafers
- Bonding to silicon carriers
- Bonding to perforated silicon (or glass) carriers
- Carrier-less system: grinding center wafer, leaving a narrow ridge at edge of wafer to maintain wafer shape ("Tyco")
  + Does not require any carrier substrate
  - Still requires protection on wafer front-side: protective tape to wafer passivation, metal pads, bumps,...
  - Non-standard post-processing
WHICH CARRIER SOLUTIONS?

- Bonding to glass wafers
- Bonding to silicon carriers:
  - our preferred solution
- Bonding to perforated silicon (or glass) carriers
- Carrier-less system: grinding center wafer, leaving a narrow ridge at edge of wafer to maintain wafer shape ("Tyco")
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3D INTEGRATION PROCESS FLOW

3D-SIC via middle

- IC fabrication line
  - Si FEOL
  - Cu nail
  - Si BEOL

Wafer Thinning module
- Wafer edge conditioning
- Temporary bonding to a Si-Carrier wafer
- Wafer thinning

Backside processing
- Cu nail exposure & backside passivation

3D-WLP via last

- Standard device wafer

Wafer debonding - Dicing - Cu-Cu or Cu/Sn µbump bonding

Backside redistribution layer & Cu or Cu/Sn µbump

Backside TSV process
IMEC’s approach to 3D-SIC*:

"Via-middle": fabrication TSV’s after FEOL device fabrication processing but before BEOL interconnect.

Key features:

- “Cu-nail” process after FEOL, before BEOL processing
- High aspect ratio Cu damascene technique
- Single litho-step

<table>
<thead>
<tr>
<th>Active Devices</th>
<th>3D-SIC/SOC</th>
<th>Interposer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer Ø</td>
<td>300 mm</td>
<td>300 mm</td>
</tr>
<tr>
<td>TSV Ø</td>
<td>5 µm</td>
<td>3 µm</td>
</tr>
<tr>
<td>TSV depth</td>
<td>50 µm</td>
<td>50 µm</td>
</tr>
</tbody>
</table>

* E.Beyne, VLSI2006, April 24, 2006 IEEE-IITC, S1P1, June 5, 2006
REQUIREMENTS TEMPORARY BONDING PROCESS

Compatible with post processing:

- Allow for excellent thickness control (TTV) after wafer thinning on carrier
WHY IS AN EXCELLENT TTV REQUIRED?

Via last:

- Thickness variation Si-substrate requires local over-etching:
  - Risk: “notching” at TSV bottom
  - Risk: Insufficient etch: Si remaining at bottom of some vias

- Therefore: Large TTV variations results in significantly lower TSV connection yield
WHY IS AN EXCELLENT TTV REQUIRED?

Via Middle: The maximum TTV corresponds to an additional depth requirement for the TSV.

- A higher depth results in a higher TSV aspect ratio requirement: e.g. achieving a 5x50 µm TSV after thinning may require 5x60µm TSV, which may require:
  - 30-40% longer etch time
  - 20% longer Cu plating time
  - Different (non-PVD) barrier and seed layer deposition

- Therefore: higher cost of ownership
REQUIREMENTS TEMPORARY BONDING PROCESS

Compatible with post processing:

- Allow for excellent thickness control (TTV) after wafer thinning on carrier

- Allow for (“low temperature” 200 - 250 °C) semiconductor processing on wafer backside:
  - Thermally stable temporary glue layer, no out gassing
  - Compatible with cassettes, loading robots, tool chucks,…

- **Easy to debond** after backside processing, preferably at low temperature without melting solder bumps
TEMPERATURE REQUIREMENTS TEMPORARY BONDING – WITH SOLDER $\mu$BUMP

$T_{\text{max}}$:

350°C (logic) down to 200°C (DRAM)

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**Temperature**

$T_{\text{max}}_{\text{device}}$  

$T_{\text{glue\_max}}$  

$T_{\text{bonding}}$  

$T_{\text{max\_backside\_process}}$

$T_{\text{solder}}$

$T_{\text{UF}}$

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Process Sequence

- Wafer thinning on carrier
- Recess etch
- Passivation
- RDL
- $\mu$bump
- Optional: $\mu$bump solder reflow
- Slide de-bonding
- Room T de-bonding
- D2W stacking using wafer-Imevel applied underfill

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PROCESSES FOR THINNING AND HANDLING OF 3D TSV WAFERS

Si (LSI) wafer

Edge trim wafer

Particle cleaning

Wafer to Carrier bonding

Wafer thinning by grinding

Grinding damage removal (Wet/dry/CMP) and cleaning

Thin wafer backside process
3D-SIC or 3D-WLP TSV process

Wafer / carrier debonding

clean & recycle carrier

Dicing thin wafer on tape

Particle clean

3D stacking

Si carrier wafer

Temporary glue layer coating

Particle clean

3D stacking
WAFER THINNING BONDED WAFER PAIR

Critical aspects:

▸ Alignment of equal size bonded wafers
▸ Fragile wafer edge of the thin wafer:

Solution:

▸ Trimming wafer edge before bonding and thinning
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EDGE INSPECTION AFTER WAFER THINNING

Carrier wafer

HT10.10

Device wafer

Microscope inspection

2

Thinned wafer

Carrier wafer
TEMPORARY GLUE LAYER DEPOSITION: CRITICAL FOR WAFER THINNING QUALITY: THIN WAFER THICKNESS VARIATIONS & DEFECTS

In film defect

- Particle
- Void

Device
Carrier

Grind

- Thinner
- Thicker

Local thickness variation on ground device wafer

Edge bead

- Device

Carrier

Bond & Grind

- Device

Carrier

Thickness variation caused by glue-layer non-uniformity over topography

Carrier

Poor planarisation over topography

- Device
- Carrier

Bond & Grind

Glue transferred to hot bond chamber walls

Carrier

Carrier

Device

Carrier

Device
USE OF IN-LINE METROLOGY DURING WAFER BONDING AND THINNING: ALLOWS FOR WAFER REWORK BEFORE THINNING

- Carrier wafer inspection (NandaTech Spark)
- Glue coat + Wafer-to-carrier Bonding
- Post-Bond SAM inspection (TEPLA SAM)
- Grinding & wet clean
- Ground Surface inspection (NandaTech Spark)
- Bonding integrity check (TEPLA SAM)
- Continue to post grinding back side processing

Rework possible
WITHIN WAFER COATING UNIFORMITY ON 300mm WAFERS

Edge bead removal is required

Optimized coating, center-to-edge <2 µm

(NandaTech Spark)
300mm WAFER THINNING PERFORMANCE ON SI CARRIER WAFERS (16µm HT1010 GLUE)

Thickness variation after thinning to 50µm

TTV = 1.6µm

ISIS measurement, 1 cm mesh,
1 cm edge exclusion

1.5µm
**BACKSIDE PASSIVATION AND Cu NAIL REVEAL MODULE**

- **Wet clean and wet Si etch to remove grinding damage**

1. **Si dry or wet etch: “via reveal”**
   - 500nm low T nitride deposition: backside passivation layer
   - Spin planarizing resist
   - Dry etch resist
   - Dry etch nitride and oxide liner

2. **Polymer deposition**
   - Spin/expose/develop
   - Polymer cure
   - Dry etch polymer
   - Dry etch nitride and oxide liner

3. **Polymer/Cu nail CMP**
   - Exposure Cu nail
WAFFER THINNING (50µm) AND BACKSIDE PASSIVATION AND CU-NAIL EXPOSURE
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WAFER DEBONDING - TOOLS @ IMEC

Suss Microtec DB12 200/300mm semi-automatic debonders

Debonding mechanism

- DB12S: Slide-debond for thermoplastic temporary glue materials

- DB12T: Peel-debond (delamination) for room temperature debondable temporary glue
SLIDE-DEBONDING OF THIN WAFERS:

Using intermediate carrier wafer to mechanically support the thin wafer:

- bond to thin wafer on carrier prior to debonding,
- Slide debond thin wafer+intermediate carrier
- Clean thin wafer on this carrier (standard spin tool)
- Debond intermediate carrier after bonding thin wafer to dicing tape

Carrier solutions:

- Electrostatic wafer carriers or vacuum wafer carriers
- Currently: limited availability
PROCESS WINDOW FOR SLIDE-DEBONDING USING HT1010 FROM BREWER SCIENCE

Peak force applied (N) on 200mm wafers during debonding

Risk of glue residues

Process window

Glue shear-regime

Sliding speed (mm/s)

Debond temperature (C)
WAFFER DEBONDING PROCESS VALIDATION OF SLIDE DEBONDING

50µm thick 300mm CMOS wafer after slide debond in Suss DB12S using a monopolar electrostatic support wafer
WAFTER DEBONDING PROCESS VALIDATION OF SLIDE DEBONDING

After slide debonding on electrostatic wafer carrier

Wet cleaning on electrostatic wafer carrier

After bonding to dicing tape

Exposed Cu nails

Grinding marks
CRITICAL ASPECTS SLIDE-DEBONDING

- Need for high temperatures is not desired in presence of solder bumps
- Sensitive wafer surface in contact to intermediate carrier
- Limited availability of suitable intermediate carrier systems
ROOM-TEMPERATURE PEEL-DEBONDING

- No temperature constraint with respect to solder bumps.
- The thin wafer is bonded to a dicing tape, prior to debonding:
  - The intermediate carrier (or stand-alone thin wafer handling) is not required
  - The sensitive surface of the backside of the thin wafer is protected by the dicing tape
- Preferred solution
- However:
  - Equivalent Si TTV capability to be proven
  - Typically requires additional process steps, additional coating materials, specific tools to prepare the surfaces for peel debonding and tools for cleaning of thin wafers on tape (non-standard tools)
THIN WAFER PEEL-DEBONDING TO DICING TAPE FRAME

50 µm thick 300mm blanket Si wafer after peel debond on tape thin wafer support in Suss DB12T
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CONCLUSIONS

- **3D-Integration technology** has three key components:
  - TSV technology
  - Wafer thinning and thin wafer carrier technology
  - Micro-bump interconnect technology for 3D

- *The wafer support system* is critical to the success of 3D system integration

- However it is *not yet fully mature*:
  - Limited set of materials and equipment available
  - Most temporary bonding materials still in development phase
REMAINING CHALLENGES

- Bonding-debonding solution for wafers with high topography, e.g. Cu-pillars or solder bumps:

  achieving planar glue layers with low TTV is required to achieve a low post-grinding TTV
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