Silicon CMOS-Integrated Nanophotonics Technology

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www.research.ibm.com / photonics
Sequoia – IBM BG/Q system

20 Petaflop; 7.9 MWatts; 96 racks; 98,304 nodes; 1.6 PB of memory;

- Multimode fiber cables, VCSEL-based transceivers
  - Each cable is a 24-fiber multimode cable, carrying 120Gbps
  - Avago Micropod transceiver (12+12) ch x 10Gbps

https://computing.llnl.gov/tutorials/bgq/
HPC driving volume optics → Computercom market

Single machine volumes similar to today’s WW parallel optics

* For max system size, availability date estimated
Optical communication for HPC

Marc Taubenblatt – IEEE Photonic Society 2011
Computer IO architecture

Von Neumann architecture of 1936

- **Cash**
- **Processor**
- **Memory**
- **Storage**
- **Network**
- **Periphery**

### Data Rates

- **PCIe**
  - 8x8Gbps → 16x12Gbps
- **XDR DRAM**
  - 7.2Gbps → 12.8Gbps
- **FC**
  - 14Gbps → 28Gbps
- **Ethernet**
  - 4x10Gbps → 4x25Gbps
- **Infiniband**
  - 12x10Gbps → 12x25Gbps
- **Firewire, USB, Thunderbolt, etc**

Requires ever increasing IO bandwidth
Monolithic Integration
Choice of technology node: Photonics scaling

Si WDM footprint

IEEE Comm. Mag., March 2012, Y. Vlasov “Si nanophotonics for Computercom beyond 100G”

90nm-65nm nodes is optimal choice for monolithic Si Nanophotonics integration
IBM Silicon Nanophotonics Technology Development

First sub-100nm technology for monolithic CMOS nanophotonics

- Provides cost-effective single-die WDM transceivers
- Scalable: dense integration, multi-channel, and multiplexing

Suitable for massive deployment covering ranges from ~cm to ~km

Take advantage of ASIC pick and place package solution

- SMF attach with passive alignment at μm precision
- Optional on die laser attach

IBM Press release, Dec 10 2012; IEDM postdeadline paper, S.Assefa et al., 2012
Silicon Integrated Nanophotonics

**DETECTOR**

**FIBER COUPLER**

**FEOL CMOS FLOW**

- Shallow Trench Isolation
- Well implants/Activation
- Gate formation
- Source/Drain Activation
- Silicidation
- Cu back-end wiring

**MODULATOR**

- Most of the mask levels and processing modules are shared
- Minimal additional photonics modules added

**Photonics as a new feature in standard CMOS**

www.research.ibm.com / photonics
Technology Design Kit – Eval Kit released April 2013

- **Main Features**
  - Base CMOS Device Pairs
    - RVt, LVt, Body Contacted RVt, Thick Ox FETS (1.8V, 2.5V, 3.3V), BC Thick Ox FETS
  - Passive Devices
    - Precision Resistors, Capacitors, Varactor, diodes, inductors, bondpads, chip guard ring
  - Transmission Lines
  - ESD Devices
    - Full suite of ESD devices supported
  - Photonics Devices
    - Waveguide, MMI Splitter, Photo Diode, Traveling Wave Modulator, WDM MUX/DeMUX, Fiber to Chip Coupler, Polarization Splitter/Rotator, Vertical Grating Coupler
  - 7 Levels of Metal … Metallurgy: 4 1x metals (M1-M4), 2 2x metals (M5, M6), 0 4x metals, LD metal

- **Tool versions used for development and test**
  - Cadence 6.1.5.507
  - MMSIM (Spectre) 11.1.0.576.ISR17
  - Calibre DRC/LVS/xRC 2013.1_27.15
  - Waveguide Path Tool
    - For drawing waveguides in layout and generating a corresponding schematic symbol for simulation.
Optical components
Silicon Modulator

- Additional mask level Si partial etch
- Doping for PN diode formation
- Shared CMOS metallization

Mach-Zehnder Silicon modulator
Electro-Optical Si Modulator – new FOM

- Define new CMOS Modulator FOM = (V\(\pi\)L)*(Loss) = (Vpp-dB)

### CMOS Modulator Loss scales with extinction ratio

- **FOM = 17.8 V-dB**
- **Vpp = 1V**
- **Vpp = 2V**

*Proposed FOM allows to assess impact on link penalty*

- 4 dB ER, 1 Vpp → 2.5 dB loss
- 10 dB ER, 1 Vpp → 5.5 dB loss
- 10 dB ER, 2 Vpp → 2.75 dB loss

**Weak carrier plasma effect**

**PIN junction carrier depletion**

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Ge Photodetector

- Dark current: 10 $\mu$A at 1V
- Responsivity: 0.7 A/W
- Bandwidth: 18GHz
- Capacitance: 20fF
Monolithic Receivers

Error-free up to 35Gbps

Power efficiency about 4pJ/bit for both designs

10Gbps

25Gbps

H.Pan et al OE 2012
Assefa et al OFC 2013

e.g. Proesel et al JSSCC 2012
4-ch WDM deMux: Double Filtering CMZ

- Fabricated using channel RX waveguides
- No additional mask levels required
- No additional processing

Experimental device performance

<table>
<thead>
<tr>
<th>Channel grid spacing (nm)</th>
<th>6.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Width of flat-top passband (nm)</td>
<td>3.8</td>
</tr>
<tr>
<td>Width of guard band (nm)</td>
<td>2.7</td>
</tr>
<tr>
<td>Crosstalk</td>
<td>&lt;25dB</td>
</tr>
<tr>
<td>Insertion loss</td>
<td>&lt;1dB</td>
</tr>
<tr>
<td>In-band ripple</td>
<td>&lt;1dB</td>
</tr>
</tbody>
</table>

• Designed for high yield
• No post-processing trimming required
• Footprint 0.6x0.3mm²
Technical feasibility demonstrated:
- Less than -25 dB crosstalk is maintained over 60°C swing
- Less than 2 dB channel insertion loss penalty over 60°C swing
WDM scaling

4ch WDM

8ch WDM

4x 6.4 ~ 26 nm

8 x3.25~27 nm
Packaging
Single Die WDM Transceiver Concept

- **Monolithic integration**: BOM cost reduction

  - Equalization of electrical link
    - Lower ASIC power
    - Smaller ASIC die

  - Retiming of electrical link
    - Reset jitter budget
    - Lower ASIC power
    - Smaller ASIC die

Y. Vlasov, IEEE Comm. Mag., February 2012
Packaging and Testing Cost Reduction

- Implementation of WDM transceiver in CMOS allows to utilize **packaging** practices of microelectronics industry

Traditional optoelectronics approach

Traditional microelectronics approach

- **Testing** practices of microelectronics industry
  - Wafer-scale testing in the middle of CMOS line
  - Wafer-scale system test at the end of CMOS line
  - Module test after packaging of best-known die

Y. Vlasov, presentation at the IEEE 802 Plenary Meeting, Hawaii, March 2012 (vlasov_01_0312_100NGOPTX)
Approach to optical assemblies

Manual assembly contributes to significant package cost
→ Need to increase degree of automation

Retire business as usual → need disruptive approach

Migration to standard ASIC packaging
→ cost reduction
Assembly route

1. Fiber ferrule
2. SiPh die
3. DFB laser array
4. Pick & Place
   Passive alignment of optical components
5. First level package
Optical Chip to Chip Links

Circa 2015

- Optical backplane: >1Tbps off-card
- Optically attached memory: >1Tbps off-module

Circa 2020

- >10Tbps off-socket IO bandwidth
- Cost-effective and power efficient IO solution

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