TSV/3D Technology Developments by ASET Japan

- Results and challenges -

July, 2013

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Agenda

• Process Technologies in ASET
  - Via-Last and C2C/W2W stacking

• Design Rules for TSV/Stacking
  - DR / KOZ / Alignments

• Demonstrators
  - 4k-I/O Memory + Logic SiP
  - CIS + Digital Sensor System
  - Non-Si RF system

- Remaining Challenges
  - Challenge List
  - Low Cost TSV

• Down-Load information
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• **Down-Load information**
Process Technologies in ASET

Via-Last for C2C

1) Attach WSS

2) Wafer Thinning

3) Deep Si Etch

4) Liner Deposition

5) Cu plating

6) Cu CMP

7) Back-side Bump Plating

8) Detach WSS/Dicing

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WSS (Glass)

Glue

SiO₂

F-Bump

Al pad

SiN

Si - sub.

TSV

B-Bump

F-Bump

Glue

Silicon
Process Technologies in ASET

4 stacked device chip using C2C platform

- One silicon interposer and four device chips.
- Successful MOSFET operation was confirmed.

(a) Bird’s-eye view

(b) cross-sectional SEM
Process Technologies in ASET

4-High stacked Slices using C2C platform

X-ray CT Scan Image
Process Technologies in ASET

Via-Last for W2W (Hybrid Bonding)
Process Technologies in ASET

Process flow and key technologies for W2W platform

1. co-planarization of copper and polymer

2. Simultaneously – formed ventilation channel

3. Pre-cleaning for hybrid copper bonding

4. Precise wafer thinning with NCG

5. Via-last TSV formation for Cu interconnect

6. B2F wafer bonding

1. Bump formation

2. F2 F bonding

3. Si thinning

4. TSV formation

5. Via-last TSV formation for Cu interconnect

6. B2F wafer bonding

7. Lithography-less TSV reveal

8. Si thinning

9. Backside ILD

10. Bonding pad

’10 FY

’11 FY

’12 FY
Pre-cleaning for W2W hybrid bonding

Hydrogen radical treatment provides both good copper-copper contact and sufficient polymer adhesion.

Sulfur SIMS profile on copper bump surface

SEM photos of bonded area
3-High Stack Wafers by W2W

- Three wafer stacking using 300 mm wafer confirms validity of the proposed process.
Process Technologies in ASET

3-High stacked Slices using W2W platform

X-ray CT Scan Image
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## TSV Targets

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>R (TSV)</td>
<td>$\leq 0.2\Omega$ (Tentative)</td>
</tr>
<tr>
<td>C (TSV)</td>
<td>$\leq 50\text{fF}$ (exclude fringe capacitance)</td>
</tr>
<tr>
<td>Via-Density</td>
<td>40k-100k via / cm$^2$</td>
</tr>
<tr>
<td>Area Penalty</td>
<td>$\leq 10$-$15%$</td>
</tr>
<tr>
<td>TSV Pitch</td>
<td>25$\mu$m</td>
</tr>
<tr>
<td>TSV Diameter</td>
<td>8-12$\mu$m</td>
</tr>
<tr>
<td>TSV Length (Via depth)</td>
<td>25$\mu$m</td>
</tr>
</tbody>
</table>

![Diagram of TSV/Stacking](image)

**Design Rules for TSV/Stacking**

ASET (Association of Super-Advanced Electronics Technologies)

July, 2013
Stacking Process Choice

<table>
<thead>
<tr>
<th></th>
<th>W2W</th>
<th>D2D</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frontside Bump</td>
<td>Cu</td>
<td>SnAg/Cu</td>
</tr>
<tr>
<td>Backside Bump</td>
<td>Cu</td>
<td>Au/Ni</td>
</tr>
<tr>
<td>Stacking Underfill</td>
<td>Hybrid</td>
<td>Capillary UF</td>
</tr>
</tbody>
</table>

Design Rules for TSV/Stacking
Design Rules for TSV/Stacking

TSV layout design

- We defined TSV layout designs for both C2C and W2W and registered to our library.

Cross-sectional view of TSV design

<table>
<thead>
<tr>
<th>Method</th>
<th>TSVΦ</th>
<th>TSV lower pad</th>
<th>Alignment margin</th>
<th>Upper window</th>
<th>Upper pad</th>
<th>TSV pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td>W2W</td>
<td>10</td>
<td>20</td>
<td>5</td>
<td>10</td>
<td>20</td>
<td>25.2</td>
</tr>
<tr>
<td>C2C</td>
<td>20</td>
<td>30</td>
<td>5</td>
<td>20</td>
<td>30</td>
<td>50.4</td>
</tr>
</tbody>
</table>
KOZ

- Evaluation of KOZ (Keep Out Zone) around TSV by measuring oscillation cycles of ring-OSCs.
  - Cycle variation less than 1% at distance of 2\(\mu\)m in C2C stacking
  - Negligible cycle variation in W2W stacking
- Current design rule defines 5\(\mu\)m margin by alignment, which is larger than the KOZ of C2C stacking. Thus, FET characteristics variations are NOT to be considered under our Via-Last process.

![Graph showing oscillation cycle variation](image)

(a) 50\(\mu\)m pitch C2C stacking

(b) 25\(\mu\)m pitch W2W stacking
Design Rules for TSV/Stacking

Alignments

Dynamic Alignment method for fine-pitch bonding (10-μm pitch, 5-μm dia.)
- High precision and in-situ alignment method, utilizing IR transmissive observation
- Up to 11,520 series bumps connected. Connection resistance: ~70mΩ/bump

Bump/Pad structures

1. Coarse alignment (reflective light)
2. Alignment at small gap (30 - 60 mm)
3. Contact shock correction
4. Alignment with solder melted

Dynamic Alignment

Resistance of daisy chains

Cross-section of joined 10 μm pitch bumps

Measurement result of daisy-chained joint
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Demonstrators

4k-I/O Memory + Logic SiP
realizing more than 100GB/sec Bandwidth with 0.56pJ/bit Power Efficiency

Cross Section SEM (C2C)

Si Interposer (Passive/Active)
Organic Interposer

SRAM
Logic
4k-I/O Memory + Logic SiP
Cross section (W2W)

SRAM

Si-IP
50µm Pitch TSV

Logic
200µm Pitch TSV
Demonstrators

4k-I/O Memory + Logic SiP (DfT)

U-Wide IO Interconnects

Memory Test

Logic Test

Data RAM

Control

Wide-Bus I/F

Data Register

Voltage Monitor

Noise Generator

Command

Reset

CLK IN

Monitor Signal

Acknowledgement

RAM Port I/F

Scan SCAN SCAN SCAN

JTAG JTAG JTAG JTAG

BIST BIST BIST BIST

4K-I/O Memory + Logic SiP (DfT)

Demonstrators
4k-I/O Memory + Logic SiP
PI/SI Monitoring by Active Interposer
Demonstrators

4k-I/O Memory + Logic SiP
PI/SI Monitoring by Active Interposer

Probe wiring

Eye diagram capture
Vdd capture
Vss capture
TSV and μBump

Logic
Si-Interposer
Memory
4k-I/O Memory + Logic SiP
PI/SI Monitoring by Active Interposer

ASET and Kobe-University made Co-design and Co-evaluation

Bandwidth = 102GB/sec
Power Efficiency = 0.56pJ/bit confirmed
Demonstrators

CIS + Digital

3D Stacked System for Automotive
(Stereo Image Sensor for Ranging)

CIS 5x5mm²
6-L Al 180nm process

CDS 5x5mm²
6L-Al 180nm process

ADC 5x5mm²
9-L Cu+Al 90nm process

IF-Chip 5x5mm²
8-L Cu+Al 130nm process
Component Development of 3D imaging sensor module

3D Stacked System for Automotive
(Stereo Image Sensor for Ranging)

The composition outline of a circuit block

Ge photo-diode for IR sensing is attached on the glass cap.

3D structure and 480 parallel operation the composition realized operation capability up-to 10,000fps.
**Requirements**

- Heat generation of image sensor 2W_{max.} \times 2, T_{jmax.} = 85\text{deg.}C, \text{Tambient}=65\text{deg.}C
- Unable to cool from the top of image sensor ⇒ **Cooling from the peripheral of Si IP**

**Overall design of image sensor**
- Cooling fins
- Objective lens
- Cu heatsink
- Heatpipe
- 3D image sensor
- Organic substrate

**Components**
- Objective lens unit
- Heatpipe
- Cu heatsink
- 3D image sensor x 2
- Si Interposer
- Organic substrate

**Cross section**
Non-Si RF system

Structure of 3D integration RF module

- Sectional view of structure
  - MEMS-SW
  - MEMS filter structure

Tunable filter ceramic substrate

- Resistive VIA
- Integrated wiring
- Raising ring
- Connecting pad

Demonstrators

Center Frequency

Bandwidth
Demonstrators

Non-Si RF system

Evaluation Board

MEMS Filter

MEMS-SW

Back Side

4.7mm

3.6mm

Control IC

Control IC
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Remaining Challenges

Challenge List

Indication of issues for TSV/3D device production (3D ASIP 2012)

- Pathfinding Tools
- WSS Improvements
- Pre/Post-Stack Testing
- Supply Chain
- Better Backside Process
- Design Tool Link to Thermal/Stress
- Cost Down
- Redundancy
- Narrow Pitch Interconnect
- Better Underfill
- Micro-bump Probing
- Warpage Control
- Fast D2D Stacking
- Non-Destructive Observation
- Removal of Overburden
- Big Die Lithography

# of Comments

0 2 4 6 8 10 12
Low Cost TSV (our trial)

We choose each element, condition of silica filler insulating layer formation and build a wafer process. TEG implementation is a silica filler of the TSV sidewall insulation and evaluation of TSV conductor.

Remaining Challenges

- **Annular Trench formation**
- **Silica filler fill**
- **Anneal (>500°C)**
- **Liquid Silica coat / Anneal**

![TEG structure diagram](image)

- **Cu paste**
- **Silica filler isolation**

**TSV Capacitance**

- **TSV insulating layer**: 4um
- **TSV capacitance**: 33fF/TSV

**Graph**

- **y = 0.033x**
- **y = 0.0356x**

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ASET (Association of Super-Advanced Electronics Technologies)
ASET’s final results of each working group were summarized into one file and uploaded to our web-site. It is a sum of presentation materials which had been presented in our Annual Accomplishment Conference (Final, March 8th, 2013). Please visit our site and download it for review.

Thank you for your attention!

Acknowledgement

This project is entrusted by NEDO “Development of Functionally Innovative 3D-Integrated Circuit (Dream Chip) Technology”
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