Precision Materials to Meet Scaling Challenges Beyond 14nm

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Continue The Lg Scaling Path

What is needed:
- Narrow fins
- Mobility enhancement
- Conductive metals
- Tunable materials
- Precision structure control

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Dennard Trend

Lg Scaling Stalled

Gated Length (nanometer)

Year

- Conventional Planar Transistor
- Thin Channel Transistor

Thin Channel Solution Path
Transistor Pathway

Si/Ge Gate All Around (GAA)
Vertical or Horizontal

Improved electrostatics
- Precision etch and CMP
- Scaled metals
- High Aspect Ratio ALD

III-V FinFET
Improved mobility
- Epi structure
- III-V gate interface
- New material CMP

Vertical TFET
Improved SS
- Epi structure
- Multi-pass CMP
- Precision etch & CMP
Precise control of materials is needed to deliver the required structure.
Precision Materials Engineering
Optimizing the material to tune in the required property

Examples from Literature

<table>
<thead>
<tr>
<th>Source</th>
<th>Modification</th>
<th>Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>J Buhler 1997</td>
<td>Phos implant into SiO2</td>
<td>HF etch rate ↑</td>
</tr>
<tr>
<td>G Tam 1989</td>
<td>H Implant into SiN</td>
<td>HF etch rate ↑, Phosphoric ER ↓</td>
</tr>
<tr>
<td>Hochbauer 2002</td>
<td>H implant into Si</td>
<td>Strain fracture</td>
</tr>
<tr>
<td>J Brugger 1997</td>
<td>Ge ion beam into Si</td>
<td>KOH etch rate ↓</td>
</tr>
</tbody>
</table>

PME Opportunities

- Implant + Etch ⇒ better control
- Implant + Anneal ⇒ material property
- Epi, CMP, Etch, ALD ⇒ precise control

Example Challenge: Spacer Width Scaling

Little margin for spacer loss from downstream cleans

Intel IEDM, VLSI 2002-2011
PME: C Addition to Spacer Improves K and Etch Ratio

Pre-epi clean exposes spacer nitride to oxide removal etch

Pre-epi clean exposes spacer nitride to oxide removal etch

Dielectric Constant K

Siconi Etch Rate Ratio to ISSG (log scale)

Applied Internal Data
Siconi Fin Recess

Si etch selectivity 100:1

<1° sidewall angle change

Smooth silicon and oxide surface

Reference  No Siconi
RMS = 0.37 nm

After Siconi
RMS = 0.34 nm

Source: IMEC/Applied Materials

Applied Internal Data
Flowable CVD Extendable Gap Fill Capability

Reentrant Structure Fill

Excellent dielectric gapfill with low thermal budget for FinFET applications
Fin Dummy Gate CMP Challenge: Stop in Film

Eliminate Dummy Gate Topology

In Situ Optical Endpoint Allows Stop in Film

In Situ Process Control on Poly CMP

Angstrom-level thickness control

Average Thickness (3mmEE)

WTW range <20Å

Applied Internal Data

Post CMP Thickness (Å)

0 1000 1050 1100 1150 1200 1250 1300 1350 1400 1450 1500

Pad Life (wafers)

0 400 800 1200
FinFET Mobility Enhancement

Replacement Stressor

Structure Design

High Mobility Channel

Replacement vs. Wrap
>50% vs. 10%

Highest-strain Si Option
70% of planar strain

Germanium Fin

Source: Applied Internal Data

Source: Penn State University

Applied Internal Data

10 nm
Precision Anneal by Millisecond Laser Treatment

Avoid Excess Dwell Temperature

Solution: low stabilization and fast cool down

Dopant Clustering with High Preheat

Cryogenic implants (Trident PTCII):
- Ge 12keV, 5E14/cm²,
- C 3keV, 5E14/cm²,
- B 0.4keV, 1E15/cm²

Soak → Laser

Architectural requirement is low stabilization temperature

NiSi Conversion interface improvement

Ref: S. Sun IWJT 2013

Chen, IEEE-RTP2009 Conference: Advances on 32nm NiPt Silicide

DSA Laser
SDE Extension Control By DSA Laser Anneal

Milliseccond Anneal & Low chuck temp

Low chuck temp & Fast cool down

**Graphs and Data**

- **Rs (Ohm/Square)**
  - DSA only
  - DSA + Spike 800C
  - DSA + Spike 900C
  - Spike 800C + DSA
  - Spike 900C + DSA

- **Implants:** B + C + GPI
  - Spike 800C
  - DSA 1200C + Spike 800C

- **B concentration (cm^-3)**
  - 1E+22
  - 1E+21
  - 1E+20
  - 1E+19
  - 1E+18
  - 1E+17
  - 1E+16
  - 1E+15

**Text**

- **DSA laser / Spike sequence simulates higher stabilization temperature**

- **Initial 800-900C exposure leads to Boron-Interstitial Cluster formation**

- **Low stabilization T+ laser anneal gives best activation**

- **Less diffusion**

**Ref:** S. Sun IWJT 2013
RMG Metal Gate Strategies

**Double Etchback**
- Tunable, band-edge
- Workfunction recess
- Conductive W fill

**Solutions**
- Tungsten Fill
  - Low $R_s$
- Trident Implant
  - Adjust Workfunction
- ALD WF
  - Tunable Workfunction
- ALD TaN etch stop
  - multiple WF metal etches
- ALD TiN / TiSiN
  - Improved Al barrier

**Workfunction as Fill**
- Conductive WF
- W fill seals seam
- Longer $L_g$ uses W fill

**Complex Integration**
- Fill 4-6nm
- 20nm $L_g$
- SAC Cap
- W Fill
- WF Cap/ES
- HiK
- Spcr

**Enabled by low $R_s$ ALD WF Materials**
Metal Fill Scaling

Below 10nm CD, thick ALD workfunction has best conductance

Gap Fill Extendibility

ALD WF fill reduces materials complexity

Fill <6nm: Poor low $L_g$ conductance

Applied Internal Data

ALD full fill solutions

CVD W with MO-TIN 3 nm + B$_2$H$_6$-W

23 $\mu\Omega$cm

ALD pWF metal

ALD nWF metal

SAC Cap

Sp cr

Cap/ES HiK

<20nm $L_g$
Metal Gate Workfunction Tuning

Objective:
reduce channel doping fluctuation

Solutions:
WF metal composition tuning

Tuning of WF metal by deposition

Effective Work Function [eV]

550mV

Alloy composition ratio varied

Tuning of WF metal by implant

Delta $V_{FB}$ [mV] from nWFM-1

Applied Internal Data

WF Metal Composition

Channel doping increases $V_t$ fluctuation:

Ref: IBM CH Lin VLSI 2012

Ref: IBM CH Lin VLSI 2012

Applied Internal Data

nWFM-2

nWFM-3

No I/I 
N I/I 2e16 
N I/I 4e16

nWFM-2

Applied Internal Data

nWFM-1
Silicide/Contact Challenge

Scalable contact fill

Interface Options:
- Silicide materials
- Implant modification and DSA anneal

Must achieve $R_c \leq 5 \times 10^{-9} \ \Omega \cdot \text{cm}^2$ to meet resistance requirements
Silicide Rc Modification

Minimize Schottky barrier
Limited by doping activation

Results from TLM
Contact resistivity (ohm-cm²)

Silicide Formation -> Implant -> DSA laser anneal for activation

Barrier reduction by P implant or Se implant with DSA activation

Ref: C.N. Ni VLSI-TSA 2013

NiPt

P I/I

Ti

CVD

Co

Ti + Se

Co + Se

Metal e

Ref: C.N. Ni VLSI-TSA 2013
Summary

FinFET scaling requires precision control of materials

- **CMP:** precision through in-situ process control
- **Dielectrics:** composition tuning
- **Junction:** optimized activation
- **Metal gate:** multi Vt by metal gate composition and implant
- **Metal gate:** improved materials to control resistance at scaled CD
- **Contact:** optimized surface doping with implant + laser anneal

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