Low-Power Error Correction For Enhanced Reliability of Flash Memories

Shiva Planjery, CEO, Codelucida, LLC
Crucial for maintaining reliability in stored data.

Necessary for meeting endurance requirements.

**TARGET CUSTOMERS**: Leading Flash controller Vendors and SSD Vendors (who build in-house controllers).
**MARKET NEED**

Estimated market size of SSDs and mobile flash storage combined ≈ $30B.

**INDUSTRY TRENDS**

- Transition from BCH (legacy solutions) to LDPC error correction to meet growing need.
  
- However, current LDPC solutions still have major issues.

**PROBLEMS IN CURRENT LDPC**

- Error floor problem: Hits a floor beyond which error-rate cannot be lowered (Target: $10^{-15}$).
  
- Larger footprint and higher power usage.
  
- Needs multiple reads to enhance reliability which affects access speeds.
KEY DIFFERENTIATORS

- New LDPC-based algorithm (different from state-of-the-art).
- Unique design approach.
- Uses low-precision computations → smaller footprint.
- Can operate with lesser reads → Faster speeds

COMPETITIVE ADVANTAGES

<table>
<thead>
<tr>
<th>FEATURE</th>
<th>BCH (Legacy)</th>
<th>State-of-the-art LDPC</th>
<th>Codelucida LDPC</th>
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<tbody>
<tr>
<td>Enhanced Reliability</td>
<td>☓</td>
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<td>●</td>
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<tr>
<td>No Error Floor</td>
<td>●</td>
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<tr>
<td>Low Power</td>
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<td>Low Chip area</td>
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<td>Low Latency</td>
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