Heterogeneous Material Integration Enabled by Advanced Wafer Bonding

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Outline

- Introduction
- Heterogeneous Material Integration
  - Full Area Wafer Level Bonding
    - Plasma Activated Fusion Bonding
    - ComBond ®
  - Wafer Level Die Transfer Bonding
- Conclusion
Introduction
Heterogeneous Integration

- Photonics
  - InP on Silicon
  - High Efficiency Detectors

- Power Devices:
  - SiC on Si,
  - GaN on Si

- Mobility enhancement solutions:
  - III-Vs to silicon
  - Ge on Silicon
  - Graphene

- Multi-Junction solar cells
Heterogeneous Integration for Silicon Photonics

UCSD

InPOI
- Wafer scale bonding of InP to SOI to produce InPOI.
- Adiabatic coupling between multiple functionally different photonic layers.

Source: UCSD

Aurrion

UC Berkeley

CMOS First Wafer Bonding
- Two step bonding of photonics layers are bonded to fully processed CMOS wafer. CMOS to SOI and III-V to SOI.
- Grating coupling between III-V active regions and the Si photonics layer.

Source: UC Berkeley

Different integration schemes are developed ➞ Most of them rely on bonding
Wafer Bonding Processes

- Direct bonding is most common for heterogeneous material integration
- Bonding with interlayers can be utilized as well for certain applications
Process Flow 1: Bulk Wafers

Incoming Wafers
- Donor Wafer
- Receiving Wafer

Surface Treatment
- Donor Wafer
- Receiving Wafer

Options:
- Almost all material combinations
- Native or deposited oxide surface

Bonding & Annealing
- Donor Wafer
- Receiving Wafer

Options:
- Plasma Activation
- ComBond®
  Alternative:
  - Bonding with interlayer

Lift Off
- Donor Wafer
- Receiving Wafer

Options:
- Splitting (up to 100x)
- Backthinning

Reuse of Donor Wafer

Value Proposition
- Significantly reduced real estate costs by wafer bonding combined with splitting
- Implementation of defect free functional layers
- Well established process similar to SOI substrates
Process Flow 2: Epitaxial Wafers

Incoming Wafers

Donor Wafer

Epitaxial layer
Substrate

Receiving Wafer

Surface Treatment

Donor Wafer

Receiving Wafer

Options:
- Almost all material combinations
- Native or deposited oxide surface

Binder

Donor Wafer

Receiving Wafer

Options:
- Plasma Activation
- ComBond
- Alternative:
  - Bonding with interlayer

Bonding & Annealing

Donor Wafer

Receiving Wafer

Options:
- Mechanical aligned bonding
- Optical Aligned Bonding

Lift Off

Options:
- Laser lift off
- Splitting
- Alternative:
  - Backthinning

Reuse of Donor Wafer

Value Proposition

- Wafer bonding enables transferring of high quality epitaxial layer on various substrates
- Reuse of donor substrate (with buffer layer) results in cost reductions
- Reduced bow and warp due to low temperature process
Direct Wafer Bonding

Plasma activated bonding
Epitaxial Growth vs. Wafer Bonding

Epitaxy

- High dislocation density
- Bowed and warped wafers

A cross-sectional TEM image of InGaAs/GaAs dislocation filter layers grown on the Si substrate.
Huiyun Liu, University of Sheffield, Photonics Society, 2013

Wafer Bonding

- No dislocations (only thin oxide layer)
- Reduced bow and warp

TEM cross section of InGaAs channel bonded to a silicon carrier
Takagi et al. VLSI Summit 2010
Direct Wafer Bonding

Epitaxial Growth Challenges
- Different lattice constant,
- Different crystal structure
- Mismatch of CTE
Difficult to overcome by process control

Direct Wafer Bonding Challenges
- Mismatch of CTE
- Surface roughness
- Cleanliness

Mismatch of CTE can result in stress which can even lead to cracks for high bonding temperatures

High surface roughness and particles result in bond defects

All parameters can be controlled!

Mismatch of CTE
Particle Voids
Heterogenous Integration

Molecular Bonding

III-V \(\rightarrow\) SOI

SiO2 deposition

CMP

Plasma activation

Bonding

State of the art:
Heterogeneous integration of light sources is key enabling for PICs

150 mm InP-to-Silicon Direct Wafer Bonding

- Low-temperature bonding process (<350°C)
- Close integration for best light coupling
- Low-cost wafer-level integration

Courtesy of J. Bowers UCSB
Plasma Activated Direct Wafer Bonding

Typical process flow for plasma activated direct bonding

- Plasma activated direct bonding enables joining of highly mismatched materials
- Fully CMOS compatible process with low temperature annealing and high bond strength

EVGs proprietary plasma activation technology is industry standard for SOI and engineered substrates

Plasma activation results in significantly reduces bond temperatures

Novel type of engineered substrates enabled by direct bonding
Direct Wafer Bonding

ComBond®
Epitaxial Growth vs. Wafer Bonding

Epitaxy

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Direct Wafer Bonding

Fusion bonding

TEM cross section of InGaAs channel bonded to a silicon carrier
Takagi et al. VLSI Summit 2010

ComBond

GaAs

TEM cross section of GaAs bonded to a silicon carrier by ComBond
EVG 2014

GaAs

- No dislocations (only thin oxide or amorphous layer)
- Reduced bow and warp

InP

10 nm

MOS interface

Bonding interface

SiO₂

Si

[001]

[110]
EVG ComBond® Platform

**Motivation**
- Fusion bonding technology is needed
  - Oxide-free Interface
  - Conductive Interface
  - Optically Transparent Interface
  - Room temperature or low temperature process
- High vacuum processing and wafer handling

**Applications**
- Heterogenous integration
- Layer transfer for advanced substrates
- Improved metal/metal bonding
- High Vacuum Encapsulation (MEMS)
EVG ComBond Platform
Processing Modules

High Vacuum Cluster
< 9x10^-8 mbar

ComBond Activation Module
Removal of Native Oxides

Vacuum Align Module
Align (<1µm) & Contact (<10kN)

Bond Module
Up to 500°C at 100kN

Bake Out Module
Surface Conditioning and Moisture Bake Out
Exemplary Results

- Silicon - Silicon Bond Interface
- GaAs - Si Bond Interface
- GaAs - InP Bond Interface*
  *Courtesy of Fraunhofer ISE
- SiC - Si Bond Interface
- SiC - SiC Bond Interface
- Al - Al Bond Interface
Wafer-Level Die Bonding
Combining Two Worlds
Wafer Size is an Issue

**Issue:**
Silicon is the best option for high volume production
Established Infrastructure

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**Source:** Nanyang Technological University, Singapore

**Wafer-level die transfer** enables high throughput and large scale integration

Implementation of InP just required with a low filling factor
- die level bonding saves material costs
- Collective die bonding saves process time
Advanced Chip to Wafer Bonding

Singulated laser dies

Flip Chip tacking of laser dies

Pre-processed photonic wafer with eutectic landing pads

Flip handle

Wafer level alignment & die transfer
⇒ Eutectic bonding using heat

Benefits:
- Only Known Good Dies
- Optimized throughput
- Various bonding processes possible
Wafer-Level Die Transfer Bonding

Plasma activation of handle populated with laser dies

Pre-processed photonic wafer with polished SiO$_2$ on top & plasma activated surface

Wafer level alignment & die transfer

Flip handle

Plasma activated direct bonding

Release of die handle

Benefits:
- Only Known Good Dies
- Optimized throughput
- **Wafer level pre-processing**
Process Results

- III-V wafer level die transfer enables 200/300mm manufacturing
- Eliminates the geometry constraints given by different wafer sizes
- High pressure uniformity enables advanced chip to wafer bonding significantly reducing process time and process costs

Source: Xianshu Luo et al., Frontiers in Materials, 28, 2015
Conclusion
Heterogeneous Integration

- Wafer bonding enables integration of III-V materials on Si
- Minimum interface thickness through direct wafer bonding
- Low temperature process

NILPhotonics™ Competence Center

- Flexible cooperation model to leverage EVG’s equipment and process know-how
- Helps to shorten time to market for innovative devices and applications.

Conclusion

Direct wafer bonding processes

- Plasma activated direct bonding
- ComBond®
- Wafer level die transfer
- 3D stacking

EVG Products

- R&D to fully automated manufacturing
- Excellent control of all critical process parameters
- Market leading performance
Thank You!