That Probe Card Costs How Much?!

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Probe Cards enabling industry innovation and test cost reduction in a relatively diminutive footprint

- Probe cards are the customization “layer” in the test cell, adapting/interfacing to each unique chip design
  - Enables broad re-use of semi-standard ATE and prober systems across many different chip designs (analogy with photomasks)
- As semiconductor functional densities continue to increase, density (+complexity) of the customization layer also increases
  - Leadtime/delivery pressure unabated, typically in the critical path of wafer-out schedules

Test Cell Spending As a % of Semiconductor Revenue

Source: VLSI Research 2016
Test Cell = ATE + Prober + Consumables
Mobile SoC Probe Complexity Increasing Exponentially
Manufactory cost-effective solutions demanding new and specialized approaches

- Adoption of advanced packaging (Copper Pillar, TSV, etc.) has driven rapid pitch reduction and a corresponding density increase
- Significant R&D and manufacturing investments required to deliver this capability, with some interesting thresholds being breached
  - 100um is diameter of a human hair, and at (beyond) positioning capability of most humans
  - Wafer fab cycle time ~45 days or ~65k minutes (manual insertion rates ~1 minute per probe)

MEMS technologies now serve >60% of advanced probe card market

Automated probe-insertion/-assembly tools in full HVM use for sub-90um pitch products
Cost Reduction Through Re-Use of Common Elements

Even in a customization layer like the probe card, some standardization can be achieved

- Printed Circuit Boards, Mechanicals, and Connectors can be up to half of probe card cost
  - Elements can be “made common” and re-used/re-cycled across multiple chip designs
  - Requires constraining probe-card design processes and segmenting/binning various tester/design combinations
- Can provide up to 20% cost-of-test reduction and leadtime reduction over full-custom scenarios