High Efficiency Power Solutions
by Chip Embedding

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Interconnections & 3D Integration

Conventional: Wire bonding & flip chip & PoP

Embedded

TSV
Embedded Technology Introduction

**Embedded Components**

- **Passive**
  - Formed
    - Resistors
  - Placed
    - Capacitors

- **Active (Die)**
  - Wafer Level Embedded Die
    - FOWLP is based on a reconfigured molded wafer infrastructure
  - Embedded Die in Substrate
    - Embedded die in package is based on a PCB type of panel infrastructure

Materials are added to the printed circuit structure to create the passive element.
The half-bridge inverter challenges

*principles and benefits of embedding*

Parasitics:
Contribute to power losses by heating

Challenges

- Limit package parasitics
- Improve thermal dissipation
- Reduce board space to get inverter closer to the appliance and thereby limit heat losses on board outside of the package

Driver chip

Half-bridge inverter

VDD

Hi-side MOSFET

Lo-side MOSFET

Load / Appliance (motor, light, A/C, induction cooker, …)

GND

GND

Load / Appliance
The half-bridge inverter challenges

principles and benefits of embedding

Miniaturization
Reduction of parasitics
# Embedded Die Substrate Technology

**aEASI - Embedded Active System Integration**

<table>
<thead>
<tr>
<th>Type</th>
<th>Schematics</th>
<th>Content</th>
<th>Status</th>
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</thead>
<tbody>
<tr>
<td>aEASI</td>
<td></td>
<td>EAP - Embedded Active Package Lead Frame based single or multi dies embedded in organic laminate material</td>
<td>1RDL 1Die passed reliability 3RDL 3Die mass production</td>
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**Diagrams:**
- **2 Layer RDL**
- **Leadframe**
- **Chip 1**
- **Chip 2**

**Module Specifications:**
- **MOSFET**: 3.4x3.0 mm²
- **DC/DC Module**: 4.5x6.6 mm²
Benefits of embedded die packaging for power inverters

- Smaller package enables
  - Board space savings
  - Close integration to the load (less parasitics for higher power efficiency)

- Better interconnections
  - Less parasitics for less heating
  - Power savings thanks to higher power efficiency

- Better thermal dissipation
  - Higher power efficiency
  - Easier to miniaturize
a-EASI Product: DC/DC Converter

- Package: 6.65 x 4.55 x 0.8 mm³, 38L
- Chip Information: 2 MOSFETs + 1 Driver Chip
- Max. average current: 60 A
- Input Voltage range: 4.5 V to 16 V
- Fast switching > 750 kHz
- Power up Blade Server
Process Flow

1. Die Attach
2. Lamination
3. Lase Drill
4. Plating
5. Pattern
6. S/M
7. ENIG
8. Laser Marking
9. Solder Printing
10. Singulation
Embedded Power Module Manufacturing

- Capacity & Yield
  - Yield = 98% in May ’16. Targeting 99% in Q4 ’16.
    - Important because of 3 KGD are embedded per device
  - Capacity of 3.3M unit/month (5x6 mm) today.
  - More than 40 M units delivered

- [Images of power module and circuit board]
aEASI - P2 Results Patent pending

Die attach  Lamination  Laser drill  Plating & Patterning  S/M, Marking, Singulation

X-Ray result
Improving the Process

P1
- Die attach AuSn TLPB
- 3 RDL layers
- Various depth vias
- Preformation of prepreg layers for lamination

P2
- Ag sintering (higher throughput and accuracy)
- 2 RDL layers
- Single depth micro vias (higher plating yields)
- Single plain prepreg lamination

→ simpler structure
→ Cost optimization
→ higher thermal dissipation
Embedded Die Power Module

- **Advantages**
  - Smaller & Thinner package
  - Excellent Thermal Dissipation
    - 2 sides cooling areas
  - Excellent Electrical Performance
    - μ-via for Gate and Source, full surface Drain
    - Low resistance & inductance, good shielding
  - Enhanced Reliability

- **Markets**
  - Power Devices, MOSFET
  - DC/DC Converter Modules
  - Fast switching Power & IGBT
Power Die - Reliability

**Power Electronic Packages**

- Al wire
  - Crack propagates through Al wire matrix
  - Increases electrical/thermal resistance

- Soft Solder
  - Crack formation in solder volume
  - Increases thermal/electrical resistance

- µ-via
  - Copper filled micro vias on Cu die pad
  - No crack expected

**Embedded Power Packages**

- TLPB / Ag Sintering
  - High melting point > 300°C
  - Stable against thermal stress
# PMIC Package Comparison

## Standard PQFN Types
- **PQFN 6x6 mm² Cu Clip**
- **PQFN 6x6 mm² Cu Wire Bond**

## Embedded Die Packages
- **aEASI 4.5x6 mm²**
- **aEASI 4.5x6 mm² cavity**
  Patent pending
PMIC Comparison - Thermal Resistance

Thermal dissipation through the PCB side

Thermal Performance
Theta Ja simulated

Thermal dissipation through the top side

Thermal Performance
Theta JTop Data Sheets

- PQFN (Cu Clip)
- PQFN (WireBond)
- aEASI (P1)
- aEASI Cavity (P2)
PMIC Comparison - Electrical Performance

RDSon contribution of the package

Series inductance of the package
Electrical & Thermal Performance

Power Efficiency

- aEASI P1
- aEASI P2
- PQFN (wire)
- PQFN (Cu Clip)

Output current (A)

Power Efficiency vs. Output current (A) for different configurations.

Diagram showing LSMOS and its components.
Embedded packaging business model

Process Flow for Embedded Devices

- Foundry
- Pre Ass'y Bump, Grind, Dice, Sort
- Embedding in Substrate
- Module Final Test
- Component Test
- Module Assembly
- OSAT Package Assembly
- Final Test
- Customer
Summary

- Embedded Components can have more and more important benefits than smaller outline
- Embedded Power Modules show advantages in Thermal and Electrical Performance
- ASE brought aEASI – Embedded Die Power Modules to HVM
- Next Gen. aEASI shows enhanced manufacturability and flexibility
Thank You

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