Advanced Packaging Enablement

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Outline

• Brief overview of SiP
• Back End Assembly Perspective (Bob Chylak K&S)
  – Tech challenges
  – Business considerations
• Front End Equipment Perspective (David Butler SPTS)
  – Tech challenges
  – Business considerations
• Summary
Many Drivers for Advanced Packaging

- Miniaturization—form factor package height, footprint
- System performance and optimization—improved signal integrity, reduced power consumption
- Heterogeneous technology integration—different device types such as RF, analog, memory
- Mixed process technology assembly—die fabricated on different silicon technology nodes
- System flexibility, features, and re-configurability
- Simplification of module level test and qualification
- Total system cost reduction, reduced development cost, faster time-to-market
Packaging Solution: SiP and FOWLP

- Smaller
- Higher Performance
- Heterogeneous
- Lower Cost
What is System in Package (SiP)?

SiP: two or more dissimilar die assembled into a standard package; can include MEMS, sensors, passives, filters, antennas; forms a functional block.
2015 SiP Market by Device Type (shares of packages shipped)

- TechSearch International estimates 13.3 billion SiPs shipped in 2015
- SiP is defined as functional system or subsystem with two or more dissimilar die, assembled into a standard footprint package
- Almost 70% of the units were RF and connectivity modules
Back End Assembly Perspective
Applications All Assembled Differently!

Source: TechSearch, Yole, TSMC, Freescale, IME, Nanium
Process Flows for the Various FOWLP Approaches

Traditional WL-FO
- Face Down Die Placement
- Metal Carrier
- Molding and Carrier Removal
- RDL and BGA Attach
- Singulation

Die First HD-FO
- RDL and Cu Pillar on Carrier
- Glass Carrier
- Face Up Die Placement
- Glass Carrier
- Molding, Thinning/Cu Via Exposure
- Glass Carrier
- RDL and BGA Attach
- Glass Carrier
- Carrier Removal

Die Last HD-FO
- RDL on Carrier
- Silicon Carrier
- Face Down Die Placement
- Silicon Carrier
- Molding
- Silicon Carrier
- Carrier Removal, RDL and BGA Attach
- Singulation


1. Face down place on film / mold / remove carrier
2. Face up heated place on film / mold / grind reveal
3. Face down thermo-compression bond
Special Requirements for SiP/FO Assembly Equipment (Compared to a Typical Flip Chip Bonder)

1. Ability to handle face up and face down placement on same machine.
2. Some processes require a heated chuck and heated place tool.
3. Most applications have multiple die in one package. Require auto tool changers.
4. Die to be bonded are presented in Tape and Reel format and from source wafers.
5. Many packages have both die and passives. So there is a desire to place passives and die on one machine.
6. FOWLP packages come in both Wafer and Panel format.
7. High accuracy or willing to trade accuracy for high productivity.
8. Equipment needs to compensate for mold shrinkage.
### Flexible vs. Optimized Machine?

<table>
<thead>
<tr>
<th>Feature</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flip and No Flip on Same Machine</td>
<td>$25K</td>
</tr>
<tr>
<td>Dynamically Heated Place Tool</td>
<td>$25K</td>
</tr>
<tr>
<td>Heated Chuck</td>
<td>$50K</td>
</tr>
<tr>
<td>Multi Die Capability</td>
<td>$25K</td>
</tr>
<tr>
<td>Tape and Reel Capability</td>
<td>$75K</td>
</tr>
<tr>
<td>High Accuracy (upward and downward camera)</td>
<td>$75K</td>
</tr>
<tr>
<td>Fan Out Machine with TCB capability</td>
<td>$75K</td>
</tr>
</tbody>
</table>
What Type of Machine for the Application?

- SMT Passives
- New SMT FC and FO
- Flip Chip
- FOW
- TCB

Accuracy (um 3sig):
- 2
- 3
- 5
- 10
- 15
- >25

UPH:
- >50K
- 10K
- 5K
- 2K
- 1K
Flip Chip Thermocompression or High Accuracy SMT/FC

TCB, Flip Chip, or FOWLP

Accuracy < 5um

Highest Accuracy 2 um
TCB 1000 to 2000 UPH
Flip Chip / Fan Out 4K – 6K UPH
High Force Capability (500N)
Heated Tool w/ TCB Capability
Strip or Wafer

SiP, Flip Chip, or FOWLP

Accuracy > 10 um

Highest Productivity
Flip Chip / FOWLP to 27K UPH
Passives to 120K CPH
Passives and Die
Panel or Wafer
Single Integrated Line for SiP
Takeaways

• Non-standardization of packaging solutions leads to highly flexible assembly equipment which drives equipment cost up.
• Industry consolidation would lead to more optimized solutions.
• New high accuracy SMT machines are an attractive solution for SiP applications.

• **Standardization and accurate roadmaps are paramount for equipment suppliers to deliver the most cost-effective machines**
Front End Equipment Perspective
SPTS: Leaders in RDL PVD for FOWLP

- 200, 300 & HD wafers
  - HVM since 2009
- Used for original eWLB development by Infineon
- Developed technology specific for FO wafers
  - Multi wafer degas – fast degas of up to 75 wafers in parallel. Essential for organic materials
  - SE-LTX – long life preclean. Up to 8,000 wafers between PM’s
  - Low Rc from in-situ pasting
- ~40% lower cost of ownership than competing systems
Multi Wafer Degas – High Throughput

FO-WLP Epoxy Mold Compound Test Vehicle, TMAX = 120C

Rvia drops as increase degas time

Individual wafers get long degas
Degas in parallel means t’put stays high

35 mins
Why We Use ICP Preclean Technology for FOWLP

Significantly Lower CO Released Using “soft” ICP Approach
• 25 um BCD, Rc data
• Wafers measured at slots 1, 6, 12, 24, 50, 100, 200 and 350
• Average ~7mohm, against spec of 30
• Not using wafer pastes in preclean during run
Simple Calculation of FO Potential – Huge Numbers

- **Apple iPhone in 2017** - ~200M phones
  - Up to 7 FO packages: AP, PMIC, CODECS, RF, switch
  - That’s 1.4B FO packages
- **Samsung in 2017** ~150M phones
  - Up to 6 FO packages = 900M
- **China phones following**
Die First or Die Last?

**Die first**
- **Advantages**
  - Lowest cost – no bump
  - Flat surface, mold to die

**Die last**
- **Advantages**
  - Die after RDL – better yield
  - No die shift

- **Disadvantages**
  - Die shift, as mold shrinks
  - Sensitive to warp
  - RDL after die – yield risk

Although yield concerns greater for die first, it is most popular. Lowest cost
The Big Question – Wafer or Panel?

- **Number of panel announcements this year**
  - PTI, SEMCO, ASE invest in Deca, IC substrate makers
  - The cost motivation is obvious – up to 6x more capacity on a panel

- **Big investments in panelFO, to fix multiple challenges:**
  - Die placement accuracy, die shift for die first
  - Material CTE mismatch, temperature swings
  - Warpage. Using glass carrier but warpage remains, and grows for more ML
  - Minimum line/space. Wafer FO approaching 2/2.

- **Economics is a tough decision**
  - >1 day to populate panel with small die, so favours large die. Yield must be >>95%
  - >$100M for a panel line, unless lucky enough to find a useable ex-display line
  - Who can fill a panel line? And who can fill the necessary second source?
  - A panel line is good for panels only. Cannot re-purpose for wafer.

Fundamentally. Panel adoption will come down to yield
RDL Inspect and Repair for PanelFO?

- **Optical inspect & repair is used in some PCB & display lines**
  - Repair RDL shorts by laser
  - Repair RDL opens by digital addition of metal
  - Typically used down to 20um line & space. 10um is current minimum

- **It’s not used in wafer level packaging lines**

- At 2016 ECTC, SPIL reported results from feasibility study on panel FO
  - 370x470 glass carrier. 10um line widths. 1 metal level
  - Yield ~15%, because of shorts/opens: incomplete RDL due to warpage, CTE mis-match, topography

- **In recent months, spike in enquiries from panelFO developers asking for RDL repair systems**
  - Asking for inspection & repair resolution 2 to 3x better than used in PCB
  - A cost adder that does not exist in a waferFO line

- **All evidence says that RDL formation is the biggest technical challenge for panelFO**
• **Fanout forecast is huge**
  – Techsearch says 87% CAGR
  – Yole forecast up to 10 new FO packages in the next marquee phones
  – Not just mobile. Automotive, medical..

• **FO on wafer is in HVM**
  – Sub 5/5 started
  – New processing technology was necessary to deal with non-Si substrates

• **Wafer or panel is the big industry question**
  – Can panel take high density FO market?

• **Significant challenges for panelFO, both technical & economic**
  – Achieving high yielding RDL is probably #1