NEXT GENERATION SILICON PHOTONICS FOR COMPUTING AND COMMUNICATION

PHILIPPE ABSIL
OUTLINE

- Introduction
- Platform Overview
- Device Library Overview
- What’s Next?
- Conclusion
DATA CENTER TRAFFIC GROWTH

Zettabyte Data Volumes

- Zettabyte/year since 2013
- Average CAGR = 32%, some reporting 50% CAGR
- >75% of this data traffic stays inside the datacenter
CLOUD DATA CENTER NETWORK
Building-wide Fiber Network

- Building-wide rack-to-rack connectivity
- Redundancy → 100,000s fiber optic links
- Up to 500m reach
- Fiber cost is substantial CAPEX
- Re-use fiber plant, upgrade optical ports

Data center network topology (Facebook)
HOW TO CONSTRUCT A **400Gbps** OPTICAL PORT?

TRANSMITTING OVER A SINGLE FIBER?

ACROSS 500m DISTANCE?

AT LOW COST (<1$/Gbps)?

AND LOW POWER (<5mW/Gbps)?

... AND HOW ABOUT **1Tbps**?
ARCHITECTURE DIVERSITY DRIVES PLATFORM AGILITY

PSM  CWDM  DWDM  SDM

Edge + Surface Couplers
Mach-Zehnder, MicroRing, GeSi Electro-Absorption Modulators
Ge Detectors
WDM Filters
OPTICAL vs. COPPER INTERCONNECTS
TRANSITION ROADMAP

Silicon Photonics as a Scalable Optical Interconnect Platform

- Datacenter [5m-10km+]
  100G-400G-1T+

- Backplane [0.5-3m]
  (N x) 50G-100G+

- Board [5-50cm]
  200Gbps+/mm

- Package or Chip [1mm-5cm]
  10Tbps+/mm

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**Copper**
- Logic Package-to-Package
- Logic-DRAM array [5cm-0.5m]

**Optical**
- Link distance
  - I/O Density
  - I/O Bandwidth

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**Source:** LightCounting

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**Backplane**
- Board-to-board [0.5m-3m]

**Intra-Datacenter**
- Rack-to-Rack [5m-500m+]
  - 1Tbps/mm
  - 100Gbps/mm
  - 10Gbps/mm

**Inter-Datacenter**
- [10km+]
  - 1.6T
  - 800G
  - 400G
  - 200G
  - 100G

**Board**
- [5-50cm]
  - 200Gbps+/mm

**Package or Chip**
- [1mm-5cm]
  - 10Tbps+/mm

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**Link distance**
- mm
- m
- km
- Mm

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**1 Gbps**
- 10G
- 50G
- 100G

**2 Gbps**
- 20G
- 40G
- 100G

**3 Gbps**
- 50G
- 100G
- 200G

**4 Gbps**
- 100G
- 200G
- 400G

**5 Gbps**
- 100G
- 200G
- 400G
- 800G

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**1 Mbps**
- 1

**2 Mbps**
- 2

**3 Mbps**
- 3

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**1 Tbps**
- 10G
- 50G
- 100G

**2 Tbps**
- 100G
- 200G
- 400G

**3 Tbps**
- 200G
- 400G
- 800G

**4 Tbps**
- 200G
- 400G
- 800G
- 1.6T

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**10 Tbps**
- 10G
- 200G
- 400G
- 800G
- 1.25G
- 2.5G
- 5G
- 10G
- 20G
- 50G
- 100G
- 200G
- 400G
- 800G
- 1.6T

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**Silicon Photonics**
- Scalable Optical Interconnect Platform

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**Optical**
- Link distance
  - mm
  - m
  - km
  - Mm
WHY SILICON PHOTONIC INTEGRATION?
Leveraging CMOS Technology

- Existing CMOS fabs with established volumes [200mm and 300mm]
- Advanced Si patterning capability [193(i), nanometer scale accuracy]
- Heterogeneous epitaxy [photodetectors/modulators]
- Low resistance contacts to Si [high-speed optical devices]
- Wafer-scale 3-D packaging and assembly [TSVs, micro-bumps, ...]
- Volume scalability [>1M units/year] & Efficiencies of scale [cost]
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ISIPP200 PLATFORM DESCRIPTION

Leveraging CMOS Technology

- Starting substrate: Silicon-On-Insulator with 220nm Si / 2000nm BOX
- 3-level Si & 1-level poly-Si patterning with 193nm lithography
- 6-level silicon doping & 2-level Ge doping
- Ge-on-Si RPCVD Epitaxy
- 2-level Cu interconnects + Al bondpad
- Deep-Si etch for edge coupling
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IMEC SILICON PHOTONICS TECHNOLOGY

**Electro-Optical Modulation Options**

**Travelling-Wave Mach-Zehnder p-n Modulator**
- 50Gb/s achieved with $2.5V_{p-p}$
- E-O Bandwidth @ $-1V_{bias}$ ~27GHz
- $V_{\pi}$ ~ 11V at quadrature, $IL_{MIN}$ ~ 2.5dB
- C-Band demonstrated, O-band designs available (similar static performance)

**Ge Electro-Absorption Modulator**
- 50Gb/s achieved with $2.0V_{p-p}$ (ER ~ 3.0dB, IL ~4.2dB)
- E-O Bandwidth @ $-1V_{bias}$ >50GHz
- Diode capacitance ~ 14fF
- Both 1615nm & 1560nm operation demonstrated

**Micro-Ring p-n Modulator**
- 56Gb/s achieved with $1.0V_{p-p}$ (ER ~ 4.7dB, IL ~3dB)
- E-O Bandwidth ~47GHz
- Transmitter Penalty @ $1.5V_{p-p}$ ~ 11dB
- C-Band demonstrated, O-band at 40Gb/s
- Diode capacitance ~20-30fF
**IMEC SILICON PHOTONICS TECHNOLOGY**

**Waveguide-Based Ge-on-Si Detectors Options**

*Typical Performance for TE at -1V, Room T., 1550nm (1310nm)*

- Device Type I: 0.85 (0.88) A/W, <50nA, >50GHz
- Device Type II: 1.0 (0.94) A/W, <50nA, 25GHz
- Device Type III: 1.15 (0.86) A/W, <15nA, 15GHz

Note: TM characteristics provided in PDK

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Device Type 2

N = 175 (3 lots, 3 masksets)
IMEC SILICON PHOTONICS TECHNOLOGY

Fiber Coupling Options

**Vertical “Raised” Grating**
- Insertion Loss to SMF-28 <2.5dB (no IMF)
- Peak-\(\lambda\) within-wafer control \(1-\sigma <4.0\)nm
- 1-dB Bandwidth ~29nm
- Both C-band & O-band available

**C-band Edge Coupler**
- Fiber-to-waveguide IL <2dB (High-NA, IMF)
- Polarization dependent loss <0.5dB
- 1dB Bandwidth >100nm
- O-Band designs in characterization
**Passive Waveguide-Based Devices**

**Waveguide Characteristics**
- SWG-WG < 2.0dB/cm, RWG-FC < 1.0dB/cm
- Thickness Control WG 3-σ < 4.5nm
- Thickness Control FC 3-σ < 10nm
- O-band described in PDK

**Waveguide-Based Filters**
- Within-device channel spacing control (2.4nm) 3-σ < 0.6nm
- Within-wafer resonator free spectral range (14nm) 3-σ < 0.25nm
- Within-wafer channel wavelength control 3-σ < 8.0nm

**Integrated Heaters**
- Two options: (1) Doped-Si, (2) Tungsten
- Standard efficiency: $P_π \sim 17\text{mW}$
- High efficiency version: $P_π \sim 4\text{mW}$ (not MPW compatible)
IMEC’S SILICON PHOTONICS PLATFORM

Fully Integrated 8x50G DWDM Si Photonics Technology

- Co-integration of the various building blocks in a single platform
- Today available on 200mm wafer size, coming soon on 300mm
- 95% compatible with CMOS130 in commercial foundries
HYBRID CMOS SI-PHOTONICS TRANSCEIVER DEMO

Putting it all together

40nm CMOS 4x20Gb/s Transceiver

28nm CMOS 50Gb/s Transmitter

Transmitter Eye Diagrams (4x20G)

Receiver Eye Diagrams (4x20G)
IMEC’S SILICON PHOTONICS OFFERING

Build your own Prototype in imec’s open platform technology!

- Accessing imec’s 200mm Si Photonics Platform (iSiPP200)
  - Both MPW and Fully Dedicated Runs
  - Silicon Validated PDK v1.3 is available
  - Supported by various EDA tools
  - >8 Customer tape-outs since 2014, >10 planned in 2016

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MONOLITHIC LASERS ON SILICON
Addressing extreme cost and performance targets

Epitaxial growth of III-V Lasers on Silicon

Wang, Nature Photonics, October 2015
INTEGRATED GRAPHENE PHOTONICS
Addressing extreme cost and performance targets

- Graphene Photonics
  - Potential for low cost [no SOI, no Ge]
  - Optical devices with wide optical bandwidth
  - Thermally robust modulators

10Gb/s eye diagram

Hu, IEDM 2014
SUMMARY

 Scaling the Cloud will require scalable optical interconnects

 imec’s Silicon Photonics Technology offers a scaling path to Terabit/s with >50-Gb/s technology at CMOS-compatible voltages ...

 ... supporting various modulation schemes & wavelength bands considered for future datacenters single-mode interconnects

 imec is your preferred Silicon Photonics development partner through its prototyping service

 Silicon Photonics’s future... based on non-silicon material
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THANK YOU!