Advanced Packaging Technologies for Miniaturized Modules

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Package Requirements

- Form Factor
- Performance
- Integration
- Low Cost
Analog Package Trends

- QFN-dr/mr
- fcQFN – FCOL/MIS
- 2L WB laminate/ 1L (Single Metal Substrate) 
- 1L WB - MIS
- 1/2L FC - MIS
- eWLB – 1L RDL

MIS can be used for leaded/laminate wirebond & flip chip packaging

eWLB drives superior performance and integration
Molded Interconnect System/Substrate (MIS)

- Carrier
- Pre-mold compound
- Surface finish: (Cu+OSP / NiAu / NiPdAu)
- Finish plating: NiPdAu, NiAu, Cu+OSP

MIS substrate 4B 250x70mm (0.11mm thickness)

Routable

External lead

Trace
MIS Process Flow

1L MIS

SPCC

1ST plating

2nd plating

Dry film stripping

Molding

OR

ABF Lamination

Top side

Grinding

Window etch/Surface finish

<table>
<thead>
<tr>
<th>Item</th>
<th>Trace/Stud</th>
<th>MIS-a</th>
<th>Cu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>ABF (LE-T178)</td>
<td>Filler Size(μm)</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Filler Content</td>
<td>82%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CTE (ppm/K)</td>
<td>Alpha1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Alpha2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Thermal Conductivity (W/mK)</td>
<td>0.65</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Young's modulus (MPa)</td>
<td>7000</td>
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<tr>
<td></td>
<td></td>
<td>Dielectric constant (DK), 5.8GHz</td>
<td>3.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Tg(deg-c)</td>
<td>DMA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TMA</td>
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</tbody>
</table>

ABF: Ajinomoto Build-up Film
Design & Application

LMIS 3.5x4.5-28L (PM Application)

- Package thickness: 0.55mm
- Lead: 0.4mm
- Pitch: 0.25mm
- Structure: Cu pillar bump with tin cap
- Bump height: 90um (65um copper + 25um solder)
- Bump size: 110um
- Material: Sn/Ag 1.8%

Cross section:

No delamination
Post MSL 1 / TCT 1500 cycles / uHAST 4
3D MIS Packaging

Characteristics
- Passive components
- Multi-chip module
- 3D MIS substrate
- Large area metal and partial fine line/space

Advantages
- Superior electrical and thermal performance
- High reliability performance

Cross section view of 3D MIS packaging

Images
- Prior electrical and thermal performance
- Reliability performance

3D MIS package for wearable communication device

Flip chip on 3D MIS

Passive components mounted on package top
**Structure:**
- Substrate thickness: 0.12mm
- Min. Bump Pitch: 90 um
- Cu column interconnect
- Molded Underfill

**Reliability Results:**

<table>
<thead>
<tr>
<th>Readout point</th>
<th>O/S test</th>
</tr>
</thead>
<tbody>
<tr>
<td>TC'B' 1000x w/ MSL3</td>
<td>SAT Image Passed</td>
</tr>
<tr>
<td>TC'B' 1000x w/ MSL2aa</td>
<td>SAT Image Passed</td>
</tr>
</tbody>
</table>

**Structure:**
- Substrate thickness: 0.11mm
- Min. Bump Pitch: 80 um
- Cu column interconnect
- Molded Underfill
**Wafer Level Packaging**

**Conventional Fan-in WLP (WLCSP)**
- Interconnect is limited to die size
- Compact package size
- Higher performance
- Lower cost than BGAs or laminate based CSPs

**Fan-out WLP (eWLB)**
- Interconnect is independent of die size
- Small package size
- Dramatically higher I/O count
- Strong thermal & electrical performance
- Able to integrate die from diverse silicon nodes
- Cost effective advanced package
eWLB provides the following capabilities:

- Small form factor
- Increased performance
- 2.5D/3D integration
- Cost effective solution

Features include:
- Fine Cu Plated RDL 5/5um LW/LS
- Ultra Thin ~0.3mm with integration
- Small form factor
- Increased performance
- 2.5D/3D integration
- Cost effective solution

eWLB provides the cost effective performance solution with increased I/O density.
FOWLP is a versatile technology platform semiconductor industry’s evolution from designs to 2.5D interposers and 3D ICs.
FOWLP breaks into New Frontiers!

- Side: Multi-die and SiP applications
  - Analog + Logic package level integration (HVM from 2012)
  - Functional partitioning
  - Large-scale side-by-side Multichip
  - Alternative solution of 2.5D Interposer

Thinner Profile

System Integration

Wide Range of SiP Offerings
Inverted FOWLP, a Disruptive Solution

Assembly Summary:

MEMS
- Individually bumped and singulated

ASIC
- Individually singulated and reconstituted with thru-vias
- Followed by backgrind, redistribution and singulation

Pre-stack:ASIC and MEMS modules pre-stack and reflow
Thank You