Heterogeneous Integration and the Photonics Packaging Roadmap

Presented by W. R. Bottoms

Packaging Photonics for Speed & Bandwidth
The Functions Of A Package

✓ Protect the contents from damage
  - Mechanical
  - Chemical
  - Electrical
  - Thermal

Photonics may be in environments we don’t contemplate today as photons get closer to the transistors in an IoT world.

✓ Provide power for operation

✓ Provide data input/output connections

✓ Do no harm
  - Latency
  - Power
  - Cost
  - Reliability

In many of these parameters packaging is the weak link.
Major Challenges

- Power
- Latency
- Thermal management
- Bandwidth density
- Cost

We must move things closer together
Photonic Component Packaging Challenges

- Low cost
- High reliability
- Use available equipment
- High bandwidth per channel
- Small size
- Low power

Near term the Roadmap is known or can be generated without significant research
Single Component Photonic Packaging

Butterfly package for laser chip used in Telecom

1. Laser chip
2. Monitor photodiode
3. Thermistor
4. Chip carrier
5. Thermoelectric
6. Lens
7. Optical isolator C
8. Component package
9. Window for light output
10. Fiber pigtail
11. Electrical leads
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What’s wrong with this picture?
- Expensive Components
- High assembly parts count
- Large size

It will not work for complex, low cost photonic systems
Replacement of these components with Integrated photonics is in process
Four Issues are Driving Change

- The approaching end of Moore’s Law scaling of CMOS
- Migration of Data, logic and applications to the Cloud
- The rise of the internet of things
- Consumerization of data and data access
Everything Must Change
Including Roadmaps

1. THE THINGS
   Products embedded with simple or smart sensors to generate data and make intelligent decisions

2. THE NETWORK
   Connecting the things to each other and processing systems in the cloud

3. THE CLOUD
   Systems that store and analyze the data to help make informed decisions

Consumer
These 4 driving forces present requirements we cannot satisfy through scaling CMOS

Lower Power, Lower latency, Lower Cost with Higher Performance

We must bring all electronics closer together and interconnect with photonics

This can only be accomplished by Heterogeneous Integration in a 3D-Complex SiP
The Network Architecture Must Change Globally and Locally

✓ Higher connectivity Flat Architecture
✓ Higher bandwidth per port
✓ Lower end-to-end latency
✓ Lower power
✓ Lower cost

Photonics to the Board, package and even chip level may be required.
The Network Architecture Must Change Globally and Locally

All this is needed at no increase in total cost and total Network power.

Power and cost/function need $>10^4$ improvement over the next 15 years.
Performance Requirements To Support This View Of The Future Network

- Higher bandwidth density
- Lower latency
- Increased data processing speed
- Expanded data storage
- Ensured reliability
- Improved security

all at no increase in cost
Performance Requirements To Support This View Of The Future Network

- Higher bandwidth density
- Lower latency
- Each of these requirements pose difficult packaging challenges
- Improved security
- All at no increase in cost
Fiber To The Board Cannot Meet The Challenge

**Today**
- Optical engines on cards optically interconnected into an electro-optical backplane

**Future**
- Optical engines on an electro-optical package substrate interconnected with system level components
Electronic/Photonic SiP through Heterogeneous Integration

Passive/IPD
-Integrated Passive Devices

Photonic Layer
-PIC Chip- optical bus

Interconnection
-Flip Chip & Wire Bond

Antenna
-Package integration for 2.4G/5G/60GHz

Molding
-MUF
-Exposed die

SMT
-Passives
-Components
-Connectors

Mechanical Assy
-Laser welding
-Flex bending

Source: ASE with additions

Packaging Photonics for Speed & Bandwidth

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Building Blocks For Integrating Photonics into SiP Exist

Optical bus

Beam splitters

Optical modulator

Laser source

Active Wavelength Locking

Ring modulator

Waveguides

WDM filters

Microbumps

Si Chip

SiHPI

Photodetector

Fiber coupler

Source: ECTC2014 Si Photonics - Stephane BERNABE with additions
Grand Challenges For Photomcis Packaging

✓ Alignment accuracy required for single mode fibers threatens yield, cost and reliability in heterogeneous integration of photonics

✓ Photonic/electronic interposer (silicon or glass) with right angle mirrors enter vias at the bottom of a PIC. Allows wafer level stacking

✓ CTE mismatch and sensitivity to temperature variation and thermally introduced stress

✓ Potential solutions modulators without temperature sensitivity and perform all “joining” processes at use case temperature
Grand Challenges cont’d

Link budget
In a complicated package link budget is the biggest optical communication limitation impacting data rate, power consumption and cost issues

Lack of a process qualification vehicle
There is cross-talk between electrical and optical data paths that contributes noise to limit limiting available link budget. Capability to simulate and verify that system operation requirements are met is needed
New Device Types Are Coming
These Devices And Their Packaging Will Use New Materials

- Carbon Nanotube Memory
  Tolerant of temp. and rad exposure
- MEMS Photonic switch
  Vertical coupler
- Spin torque devices
  (2 magnetic junction pillars)
- Plasmonic emission Source
  (quantum dots and plasmons)
- Plasmons in CNT Waveguide
  1000 x smaller than photon
- GaAs nanowire lasers
  (grown on Si with waveguides embedded)
Co-Integration of Technologies

Use each technology where it is the best:

✓ Electronics
  – Active logic and memory (Processing and routing)
  – Smallest size

✓ Photonics
  – High bandwidth
  – Energy efficient
  – Long and intermediate distance

✓ Plasmonics
  – Much smaller than photonic components
  – Potentially seamless interface between Optics and Electronics
  – Low power active functions
How Do We Test SiP Electronic-Photonic products?

✓ Integrate Optical Ports to Provide Access to Test Optical IPS Functions
  – Optical Sources to Generate Test Light Beam
    • Multiple Beams
    • Wavelength
    • Power Level
    • Modulation Method
    • Polarization
  – Suitable Detectors required
    • Multiple Detectors
    • Wavelength
    • Sensitivity
    • Bandwidth
    • Skew Detection
  – Coupling Methods
    • From/To Fiber/Fibers
    • From/To Waveguide/Waveguides
    • From/To “Free Space”

✓ Mix with Electronic Test Points
How Do We Test SiP Electronic-Photonic products?

✓ Integrate Optical Ports to Provide Access to Test Optical IPS Functions

These components are complex with many parameters to be tested. It is **not sufficient** to test only before shipment. Transistors in the system wear out and photonic components may drift in wavelength.

**We must have intelligent redundancy, continuous test while running, dynamic self repair and graceful degradation if we want reliable systems.**

- From/To Waveguide/Waveguides
- From/To “Free Space”

✓ Mix with Electronic Test Points
## What Limits Rate Of Progress

### We have:
- ✓ Components
- ✓ Materials
- ✓ Processes
- ✓ Designs
- ✓ Prototype parts

### We don’t have:
- ✓ High volume markets
- ✓ Photonic specific production/assembly equipment
- ✓ High volume production to come down the learning curve

We need product(s) based on equipment and materials we have and physics that is understood that can be delivered in 12-18 months to demonstration the known cost and performance advantages of integrated photonics.
Low Hanging Fruit

Optical oxygen concentration sensor
A small, low cost wearable patch that can sense through the skin and report using connection to smartphone. Can be disposable. Additional optical sensors may be added for other chemicals.

Fiber-optic connection as a sensor
The optics developed for chemical/biological sensors may be used as a low cost method for monitoring the performance of photonic circuits
Low Hanging Fruit

**Lidar device**
A small, low power LIDAR with characteristics that would support use in very high volume, low cost applications.

**Large port count multi-channel receiver**
Reduced energy and space with competitive performance. All the components exist and only need to be integrated and packaged.

Ideal “low hanging fruit” devices can be integrated with CMOS logic and memory through heterogeneous integration into future complex electronic/photonic SiP products
Summary

New driving forces are increasing the demand for innovation in Heterogeneous Integration and Photonics Packaging

✓ We have the components
✓ Co-design and simulation tools are maturing
✓ Progress will be paced by how aggressive we are in integrating these assets into high volume products with lower cost, reduced power, reduced latency, higher performance, and smaller size

Roadmaps can enable pre-competitive collaboration to reduce cost and time to market.
Thank You for Your Attention